

QDD-800G-2DR4

QSFP-DD 800G 2xDR4 2x400Gbps PAM4 500m, 1310nm 3dB Dual MPO12/APC SM

1. Product overview

800G QSFP-DD optical transceiver for single-mode fiber, with MTP/MPO-12 connectivity and a reach of 500 m. Eight parallel optical lanes support 800G transmission, 2x400G DR4 or 8x100G DR breakout. Built-in digital diagnostics provide access to real-time operating parameters.

2. Key features

Hot-pluggable QSFP-DD; 8 electrical lanes; 16.5 W maximum; CMIS 5.0; two-wire serial interface with digital diagnostic monitoring; 0 to 70°C case temperature. QSFP-DD MSA Type 2A with MPO-16 connector.

3. Applications

800G Ethernet; data centers; 2x400G DR4 or 8x100G DR breakout.

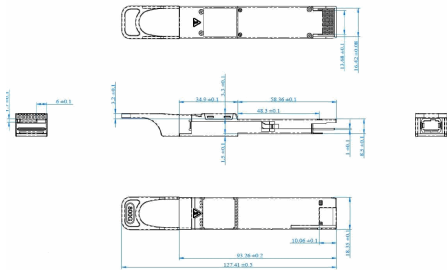
4. Technical data

Absolute maximum ratings	Value	Absolute maximum ratings	Value
Storage temperature	-40 to +85°C	Supply voltage	-0.5 to 3.6 V
Relative humidity	5-95%, non-condensing	Differential data input	1 V max
Control input voltage	-0.3 to Vcc+0.5 V	Control output current	-20 to +20 mA

High-speed electrical characteristics - IEEE 802.3ck C2M; TP1/TP1a module input, TP4 module output.

Module input	Specification	Module output	Specification
Differential input tolerance	750 mV p-p min	Differential output, p-p	600 / 845 mV max (short / long)
AC common-mode tolerance	25 mV RMS min	AC common-mode output	25 mV RMS max
Differential-to-common return loss	802.3ck 120G-2 (dB)	Common-to-differential return loss	802.3ck 120G-1 (dB)
Effective return loss	8.5 dB min	Effective return loss	8.5 dB min
Termination mismatch	10% max	Termination mismatch	10% max
Single-ended tolerance	-0.4 to 3.3 V	Eye height / vertical eye closure	15 mV min / 12 dB max
DC common-mode tolerance	-0.35 to 2.85 V	DC common-mode / transition	-0.35 to 2.85 V / 8.5 ps min

Mechanical drawing - units not explicitly stated in source.



Simplified functional illustration



Module pin mapping and low-speed electrical limits are listed on page 2.

Source host schematic: 3.3 V; three 1 μ H supply inductors; 4.7 k Ω to 10 k Ω SCL/SDA pull-ups and a 1.0 k Ω pull-up. Filter capacitors are informative/application-dependent; 0.1 μ F capacitors close to power pads may be duplicated. Vcc1/Vcc2 may connect to TX or RX supplies subject to maximum-current derating.

5. Recommended operating conditions

Parameter	Specification	Parameter	Specification
Case temperature / supply	0-70°C / 3.135 / 3.3 / 3.465 V (min/typ/max)	Lane speed / TWI clock	53.125 GBd typ / 400 kHz max
Peak hot-plug current	TBD in source	Sustained hot-plug current	TBD in source
Power / low-power max	16.5 W / TBD	Supply noise, 1 kHz-1 MHz	66 mV p-p max
Control high / low	0.7Vcc to Vcc+0.3 V / -0.3 to 0.3Vcc V	Operating distance	2-500 m

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6. Optical characteristics

Transmitter	Specification	Receiver / stress conditions	Specification
Wavelength, min / typ / max	1304.5 / 1311 / 1317.5 nm	Wavelength, min / typ / max	1304.5 / 1311 / 1317.5 nm
SMSR	30 dB min	Damage threshold / lane	5 dBm min
Average launch power / lane	-2.9 to +4 dBm	Average receive power / lane	-5.9 to +4 dBm
OMAOuter / lane	-0.8 to +4.2 dBm	Receive OMAouter / lane	4.2 dBm max
OMAOuter minus TDECQ / lane	-2.2 dBm min (ER ≥5 dB); -1.9 dBm min (ER <5 dB)	Receiver reflectance	-26 dB max
TDECQ / lane	3.4 dB max	Receiver sensitivity OMAouter / lane	max(-3.9, SECQ - 5.3) dBm max
TDECQ - 10log10(Ceq) / lane	3.4 dB max	Stressed RX sensitivity / lane	-1.9 dBm max
TX-off average power / lane	-15 dBm max	SECQ, lane under test	3.4 dB typ
Extinction ratio / transition	3.5 dB min / 17 ps max	SECQ - 10log10(Ceq), lane under test	3.4 dB typ
RIN15.5OMA	-136 dB/Hz max	OMAOuter, each aggressor lane	4.2 dBm typ
Optical return loss tolerance	15.5 dB max		
Transmitter reflectance	-26 dB max		

Minimum average TX launch power is informative, not the principal signal-strength indicator. TX reflectance is defined looking into the transmitter. Stressed sensitivity: conformance signal at TP3, BER 2.4x10⁻⁴. Receiver sensitivity is informative, defined for transmitter SECQ up to 3.4 dB. Stress-test values describe the test signal, not receiver operating limits.

7. Digital diagnostics and management

Internally calibrated: temperature 0-70°C, ±3°C; voltage 0-Vcc, accuracy 0.1 V; per-lane bias 0-100 mA, 10%; TX power -2.9 to +4, ±3; RX power -5.9 to +4, ±3 (source optical-monitor unit: dB).

Low-speed electrical signals	Limits (min to max)
SCL/SDA output / input	VOL 0-0.4 V; input VIL -0.3 to 0.3Vcc V; VIH 0.7Vcc to Vcc+0.5 V
InitMode, ResetL, ModSelL	VIL -0.3 to 0.8 V; VIH 2 to Vcc+0.3 V
IntL	VOL 0-0.4 V; VOH Vcc-0.5 to Vcc+0.3 V

76-pin map (p/n pairs, lanes 1-8): TX CML-I: 36/37, 3/2, 33/34, 6/5, 74/75, 41/40, 71/72, 44/43. RX CML-O: 17/18, 22/21, 14/15, 25/24, 55/56, 60/59, 52/53, 63/62. 3.3 V supplies: RX 10/48; TX 29/67; Vcc1/2 30/68. LVTTTL inputs: select 8, reset 9, low-power/optional TX-disable 31; outputs: presence 27, interrupt/optional RX-LOS 28. SCL/SDA 11/12: LVCMOS-I/O. Vendor-specific P/V/S4/1 inputs 46/47 and P/V/S2/3 outputs 49/50: LVCMOS/CML. ePPS/Clock 69: LVCMOS-I, 1PPS PTP/reference clock. 65 NC; 66 reserved. All other pins GND.

8. Safety and regulatory

IEEE 802.3cu-2021: 8x100GBASE-DR; IEEE P802.3ck D3.0: 8x100GAUI-1 C2M; QSFP-DD MSA HW 6.01 Type 2A MPO-12; CMIS 5.0; EU 2011/65/EU; Class 1 laser.

9. Ordering information

Original part number	Description
QDD-800G-2DR4	QSFP-DD 800G 2xDR4 2x400Gbps PAM4 500m, 1310nm 3dB Dual MPO12/APC SM