QDD-400G-VR4

Source product: QSFP-DD-VR4-400G | 850 nm | 50 m OM4 | MPO-12 APC

1. Product overview

The supplied file describes a hot-pluggable QSFP112 400GBASE-VR4 transceiver with four 100G PAM4 VCSEL lanes and PIN receiver. It transmits and receives up to 106.25 Gb/s per lane over multimode fiber; features and ordering specify 50 m OM4.

2. Key features

400G Ethernet / QSFP112 MSA; 4x100G PAM4 VCSEL array; MPO-12 APC; single 3.3 V supply; DDM; maximum power 9 W; operating case 0 to 70°C; Class 1 laser.

3. Applications

400GBASE-SR4 Ethernet; InfiniBand NDR; switch/router connections; Data Centers; other 400G interconnect requirements.

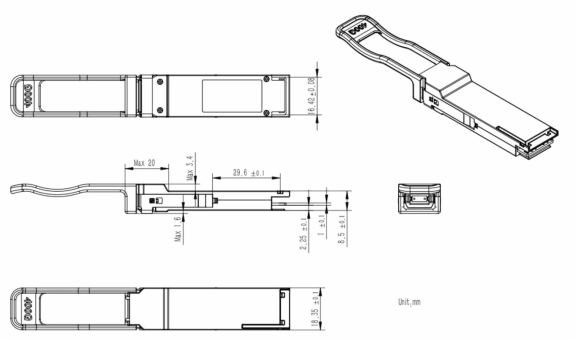
4. Technical data

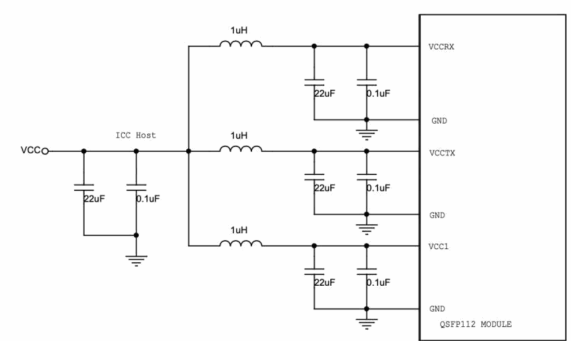
Parameter	Specification	Parameter	Specification
Source form factor / optical interface	QSFP112 / MPO-12 APC	Storage / relative humidity	-40 to +85°C / 5-95%
Source lane rate / detector	106.25 Gb/s PAM4 / PIN	Absolute supply voltage	-0.5 to +4.0 V
Power / supply current	9 W max / 3000 mA max		

Electrical characteristics

Parameter	Specification	Parameter	Specification
Electrical supply range	3.14-3.47 V	RX single-ended output voltage	0.45 V max
TX / RX PAM4 rate per lane	53.125 GBd typ	RX differential output swing	900 mV p-p max
TX single-ended input tolerance	-0.3 to +4.0 V	Power-on initialization time	2000 ms max
TX differential input swing	880 mV p-p max	IIC fast clock / clock stretching	1 MHz max / 500 µs max
TX / RX common-mode noise RMS	17.5 / 17.5 mV max	IIC data hold time	300 ns min
TX / RX termination mismatch	10 / 10% max		

Source mechanical drawing and recommended host supply filter





MPO-12 lane sequence (source view, key up): TX1, TX2, TX3, TX4; four unused center positions; RX4, RX3, RX2, RX1.

5. Recommended operating conditions

Parameter	Specification	Parameter	Specification
Case temperature	0 to +70°C	Supply voltage (min/typ/max)	3.135 / 3.3 / 3.465 V

Simplified functional illustration

4 PAM4 lanes	VCSEL / PIN	4 optical lanes	MPO-12 APC / MMF

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6. Optical characteristics

Transmitter (per lane where stated)	Specification
Signaling rate, per lane	53.125 ±100pm GBd
Modulation	PAM4
Center wavelength (min/typ/max)	844 / 850 / 860 nm
RMS spectral width	0.6 dB max
Average launch power, each lane	-4.6 to +4 dBm
OMAouter, each lane	-2.6 to +3.5 dBm
Transmitter excursion, each lane	2.3 dB max
TDECQ, each lane	4.4 dB max
Average launch power, OFF / lane	-30 dBm max
Transmitter transition time	17 ps max
Optical extinction ratio	2.5 dB min
RIN12OMA	-132 dB/Hz max
Optical return loss tolerance	12 dB max
Encircled flux	≥86% at 19 mm; ≤30% at 4.5 mm

Receiver / stressed test	Specification
Signaling rate, per lane	53.125 ±100pm GBd
Modulation	PAM4
Operating input wavelength	842-948 nm
Damage threshold, each lane	5 dBm min
Average receive power, each lane	-6.4 to +4 dBm
Receive OMAouter, each lane	3.5 dBm max
Receiver reflectance	-12 dB max
Sensitivity (OMAouter), each lane	-4.6 dBm max
Stressed sensitivity (OMAouter)	-2 dBm max; BER 2.4E-4, TDECQ 4.4

7. Digital diagnostics and management

Function	Source specification
Digital diagnostics / management	DDM implemented; two-wire IIC interface, SCL 11 / SDA 12. No diagnostic accuracy limits or CMIS revision are stated. Memory-map figure in source is marked DRAFT.
Memory map: lower / bank-independent	Lower page 00h: module dynamic information; 7Eh bank select / 7Fh page select. Upper 80h-FFh: 00h system ID/advertisement, 01h revision/wavelengths, 02h module/lane thresholds, 03h user EEPROM; 04h-0Fh reserved; 20h-7Fh reserved for coherent; 80h-AFh custom. Bank-independent NVR data does not change with bank select.
Memory map: bank-dependent	Banks 0-3, pages 10h-1Fh: lane dynamic information. 10h channel control/masks; 11h channel state/flags/monitors; 12h diagnostics; 13h-15h WDM/FEC control; 16h-17h reserved for coherent; 18h-1Dh reserved; 1Eh-1Fh custom.
Supply / filter notes	VccRx, Vcc1 and VccTx applied concurrently, may be internally connected; contact current 1.5 A max (2 A for 15-20 W modules, as source generic note). Filter inductors DC resistance <0.1 ohm. Filter voltage drop counts against host DC set-point accuracy.

Pin assignment / interface notes: Source pin list (through 51 only): TX p/n lanes1-4:36/37,3/2,33/34,6/5; lanes6/8:41/40,44/43. TX pins3/6/41/44: non-inverted outputs;33/36: inverted inputs;34/37: non-inverted outputs;2/5/40/43: inverted inputs (all source CML-I). RX p/n lanes1-4:17/18,22/21,14/15,25/24 (CML-O). GND1,4,7,13,16,19,20,23,26,32,35,38,39,42,45,51 common to host plane. VccRx10,VccTx29,Vcc1 30,VccRx1 48. ModSelL8,ResetL9,ModPrsL27,IntL/RxLOS28,LPMode/TxDis31. Reserved46;VS1/2/3=47/49/50.

8. Safety and regulatory

Class 1 laser; RoHS compliant (ordering table).

9. Ordering information

Product / file identifier	Description
QDD-400G-VR4	QSFP-DD 400G-VR4 4x100Gbps PAM4, 850nm 1.8dB 50m MM MPO12/APC